A capacitorless 1T-DRAM technology using gate-induced drain-leakage (GIDL) current for low-power and high-speed embedded memory

doi: 10.1109/TED.2006.870283

A Capacitorless 1T-DRAM Technology Using Gate-Induced Drain-Leakage (GIDL) Current for Low-Power and High-Speed Embedded Memory

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***Abstract*—A capacitorless one-transistor (1T)-dynamic random-access memory (DRAM) cell using gate-induced drain-leakage (GIDL) current for write operation was demonstrated. Compared with the conventional write operation with impact-ionization (II) current, the write operation with GIDL current achieves power consumption that is lower by four orders of magnitude and a write speed within several nanoseconds. The capacitorless 1T DRAM is the most promising technology for high-performance embedded-DRAM large-scale integration.**

***Index Terms*—Dynamic random-access memory (DRAM), embedded memory, floating-body effect, gate-induced drain leakage (GIDL), silicon-on-insulator (SOI).**

I. Introduction

THE DEMAND for large-capacity high-speed low-power embedded memories has been increasing. There are normally two kinds of memory, namely, embedded static random-access memory (SRAM) and embedded dynamic random-access memory (DRAM). Although the former can operate at very high speeds, it occupies a large area on the large-scale integration (LSI) because of its six-transistor (6T)-cell structure. Moreover, it is becoming difficult for an embedded SRAM to be scaled down because of the problem of matching between cell transistors. An embedded DRAM, which consists of one transistor and one capacitor (1T/1C), has a small cell size and a high operation speed. However, it requires a complicated stack capacitor or a deep-trench capacitor in order to obtain a sufficient storage capacitance (around 30 fF/cell) in smaller cells. This leads to more process steps and, consequently, less process compatibility with logic devices.

In light of this situation, several reports about another kind of embedded memory, called a capacitorless 1T DRAM or a floating-body cell (FBC), have been published [1]–[10]. This new memory cell uses a floating-body of a partially depleted (PD) silicon-on-insulator (SOI) MOSFET as a storage node. Therefore, the 1T DRAM does not need a complicated storage capacitor, and this means that the cell has a good process compatibility with logic devices. The features of these embedded memories are summarized in Table I [7]. Considering the capacity, the speed, and the structural complexity of an embedded memory, a capacitorless 1T DRAM is an attractive technology for a high-performance embedded-DRAM LSI.

TABLE I
FEATURES OF THE 1T DRAM VERSUS OTHER EMBEDDED MEMORIES

	DRAM	SRAM	1T-DRAM
Cell size	$8F^2$	$100F^2$	$4F^2$
Cell complexity	1T1C	6T	1T
Store mesh	Capacitor	Flip flop	Floating body
New material	High-k	None	None
Speed	fast	Ultra fast	fast
Read	destroy	Non destructive	Non destructive

The 1T-DRAM cells presented in [1]–[7] and [10] use impact-ionization (II) current for write operations. A higher writing speed would require an increase in II current. This leads to an increase in power consumption due to the large drain current. This paper proposes a design of a 1T-DRAM cell that utilizes gate-induced drain-leakage (GIDL) current for write operations and describes characteristics of the resultant low-power high-speed operation.

II. Mechanism of Memory Operations Using GIDL Current

Fig. 1 schematically shows the operation principle of a 1T-DRAM cell. The cell senses whether the majority carriers (holes) accumulate in the floating-body as the threshold voltage ($V_{\rm th}$) changes. The source is set to 0 volt, the drain is connected to a bitline (BL), and the gate is connected to a wordline (WL). When excess holes exist in the floating-body and $V_{\rm th}$ lowers, the cell state can be regarded as "1." On the other hand, when excess holes are swept out of the floating-body by a forward bias on the body–drain junction and $V_{\rm th}$ becomes higher, the cell state can be regarded as "0." The drain-current difference between "1" and "0" states can be sensed in the linear current region so as not to change the number of holes by the II current. By performing a read operation in the linear current region, the 1T-DRAM cell achieves the nondestructive read operation during a refresh interval.

The structure of the 1T-DRAM cell is the same as a conventional PD SOI MOSFET. Therefore, the origin of GIDL current in the 1T-DRAM cell is identical to that in the PD SOI MOSFET [11]. The GIDL current originates from band-to-band

Manuscript received June 13, 2005; revised November 30, 2005. The review of this paper was arranged by Editor S.-I. Kimura.

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Digital Object Identifier 10.1109/TED.2006.870283

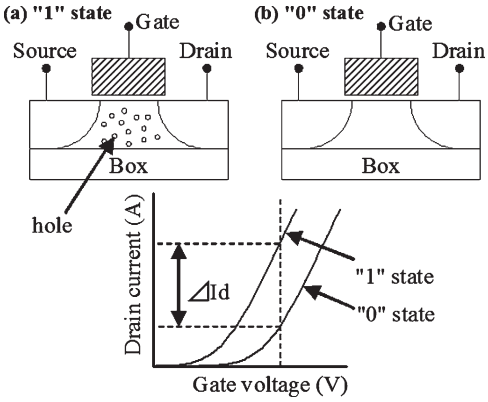


Fig. 1. Principle of 1T-DRAM cell. (a) Body region accumulates holes, which leads to a lower $V_{\rm th}$. (b) Holes are not accumulated.

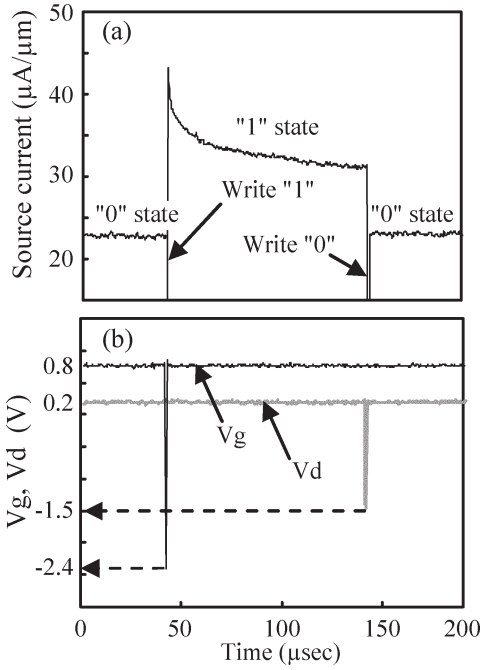


Fig. 2. Relationship between the source current and the time for write "1" operation using GIDL current: (a) source current and (b) applied voltage. After the write "1" operation, the source current increases since generated holes accumulate in the body. The write "0" operation sweeps out the accumulated holes; then, the source current decreases.

tunneling of electrons and occurs in the gate–drain overlap region during application of a negative voltage to the gate and a positive voltage to the drain. At the same time, as the tunneling electron flows to the drain, the generated hole flows to the floating-body and accumulates there. Write "1" operations using GIDL current and write "0" operations were verified experimentally. Fig. 2 shows the relationships between the source current and the time for a write "1" operation using GIDL current, with the time-dependent change of the gate and drain voltage. A digital oscilloscope was used to measure the source current. Device parameters for SOI nMOSFETs in this paper are as follows: $L_g = 200$ nm; $T_{\rm si} = 70$ nm; $T_{\rm ox} = 5.8$ nm; and $T_{\rm box} = 150$ nm. After the write "1" operation with a gate voltage of -2.4 V and a drain voltage of 0.2 V, the source current increases because of accumulated holes in the body and the resultant threshold-voltage change.

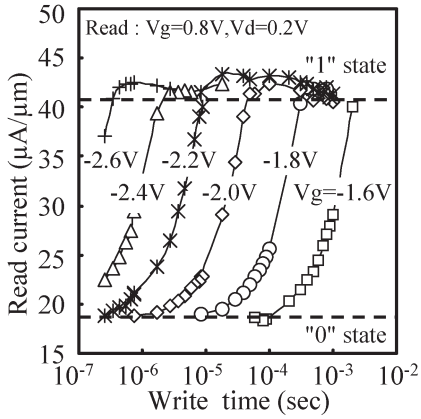


Fig. 3. Dependence of the read current on the write "1" time having different gate voltages at a drain voltage of 0.2 V. For example, a write time of 10^{-5} s is necessary for write "1" at a gate voltage of -2.2 V.

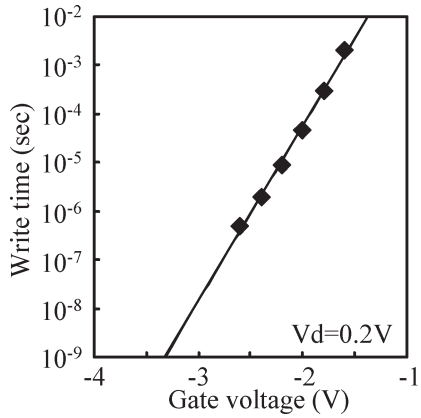


Fig. 4. Write "1" time versus the gate voltage required for write "1." The write "1" time becomes shorter as the gate voltage decreases because the GIDL current increases.

After the write "0" operation with a gate voltage of 0.8 V and a drain voltage of -1.5 V, the source current decreases because of the lack of holes in the floating-body as a result of the forward bias on the p-n junction consisting of the body and the drain.

III. Memory Operation Characteristics

A. Write Speed

Fig. 3 shows the dependence of read current on the write "1" time having different gate voltages at a drain voltage of 0.2 V. The write time is the gate pulsewidth for the write "1" operation, and the read current is the source current after a gate pulse application. We defined a read current of 20 μA/μm for the "0" state and any source current more than 40 μA/μm for the "1" state.

The time required for write "1" becomes shorter as the gate voltage becomes negatively large. This is because the GIDL current increases as the voltage difference between the gate and the drain becomes larger. Especially for the 1T-DRAM cell, the body voltage follows the gate voltage because the body is electrically floating. As a result, band-to-band tunneling current increases in accordance with the large lateral electric field between the body and the drain. Fig. 4 shows the relationship

TABLE II
COMPARISON BETWEEN WRITE "1" POWER CONSUMPTION FOR II CURRENT AND THAT FOR GIDL CURRENT

	Drain current during write "1" operation	Power consumption for write "1" operation
GIDL	1.5 x 10^{-8} A/μm	2.4 x 10^{-8} W
I.I.	2 x 10^{-4} A/μm	3.2 x 10^{-4} W

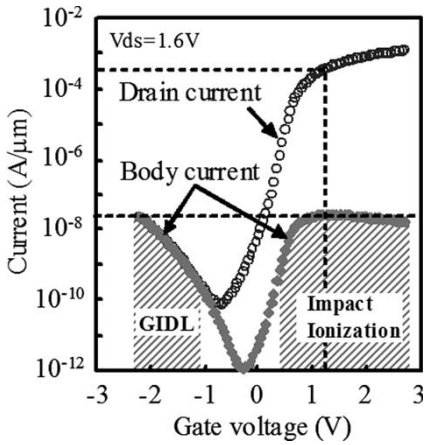


Fig. 5. Dependence of the drain and the body current on the gate voltage. The drain current where GIDL current is used to write "1" state is lower than that where II current is used, which leads to a reduced power consumption.

between the write "1" time and the applied gate voltage at a drain voltage of 0.2 V. The results indicate that write operation speeds in the nanosecond range can be obtained by applying −3.3 V to the gate at a drain voltage of 0.2 V. In other words, data "1" can be written in nanoseconds with a voltage difference of 3.5 V between the gate and the drain.

B. Power Consumption

The power consumption of the write "1" operation can be dramatically reduced if GIDL current is used instead of II current. Table II compares the power consumption between cases where either GIDL current or II current is used in the write "1" operation under the same write speed of nanoseconds. For the GIDL case, the voltage difference of more than 3.5 V between the gate and the drain is needed to obtain the write "1" speed in nanoseconds. In order to compare under the same write speed and the same drain voltage, we used a drain voltage of 1.6 V for both the GIDL case and the II case. The difference in power consumption can be attributed to a difference in the drain current during the write "1" operation as shown in Fig. 5. Since the GIDL current originates from band-to-band tunneling, which means the tunneling electron flows to the drain and the generated hole flows to the floating-body, the drain current is the same as the body current during the write "1" operation.

C. Sense Margin

The difference in the drain current between the "1" state and the "0" state becomes larger when the GIDL writing

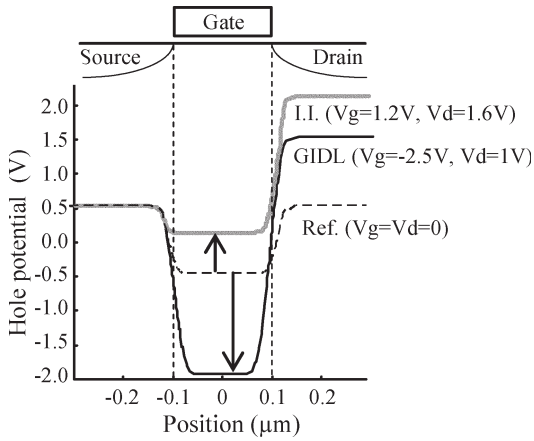


Fig. 6. Hole potential immediately after the voltage of the write "1" operation is applied.

condition is used, which leads to a large sense margin in data read operations. The two-dimensional device simulation was performed to compare the body potential between cases where either GIDL or II current is used. Device parameters used for the simulation are similar to that of the experimental device and are as follows: $L_g = 200$ nm; $T_{\rm si} = 70$ nm; $T_{\rm ox} = 5.8$ nm; and $T_{\rm box} = 150$ nm. The simulation was performed using the two-dimensional device simulator MEDICI.

Fig. 6 shows simulated results of the hole potential in cases where either GIDL or II current is used just after application of write "1" voltages. In order to compare both the write "1" method under the same write speed in the nanosecond range, write "1" voltages are selected so as to generate the same body current. For a GIDL case, a gate voltage of −2.5 V and a drain voltage of 1 V are used. For the II case, a gate voltage of 1.2 V and a drain voltage of 1.6 V are used. For the GIDL case, the body potential becomes negatively large because of the capacitive coupling between the body and the gate. This body potential leads to an increase in the number of accumulated holes because the barrier height between the body and the source becomes higher than that for the II case. Fig. 7 shows a comparison of simulated read-current and body-voltage changes during the write "1" and read "1" operations using GIDL current and II current. We had previously defined a source current of 20 μA/μm for the "0" state and any source current more than 40 μA/μm for the "1" state. Therefore, the sense margin can be regarded as the source current minus 20 μA/μm. The source current of the "1" state became larger in the GIDL case than in the II case, which means that there was a larger sense margin in the GIDL case. A larger body voltage of 0.13 V and resulting higher read current of 12 μA/μm can be observed for GIDL current.

IV. CIRCUIT DESIGN CONSIDERATIONS

The operating-voltage conditions for the 1T-DRAM cell using GIDL current are summarized in Table III. The voltage of the write "1" operation is determined so that a writing speed of a few nanoseconds is achieved. Other voltages are similar to conventional conditions [10]. Fig. 8 simulates sequential voltage changes for each node, such as the gate,

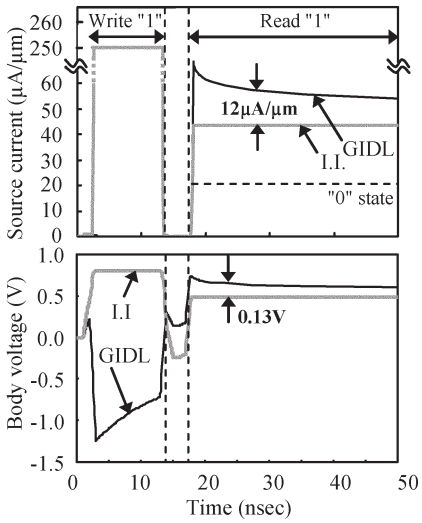


Fig. 7. Comparison between simulated read "1" current after the write "1" operation using II current and that after the write "1" operation using GIDL current.

TABLE III
MEMORY OPERATING-VOLTAGE CONDITIONS

	Write "1"	Write "0"	Read	Hold
Gate voltage (V)	-2.5	0.8	0.8	-1
Drain voltage (V)	1	-1.6	0.2	0

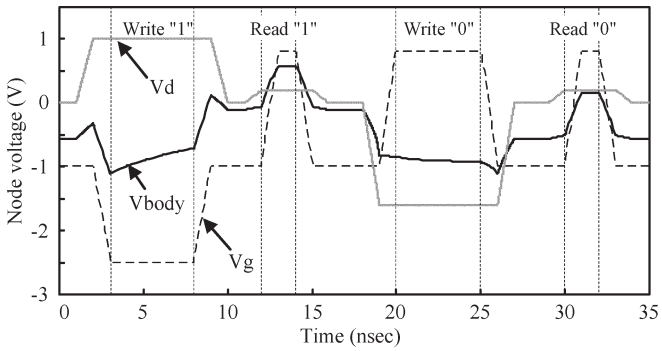
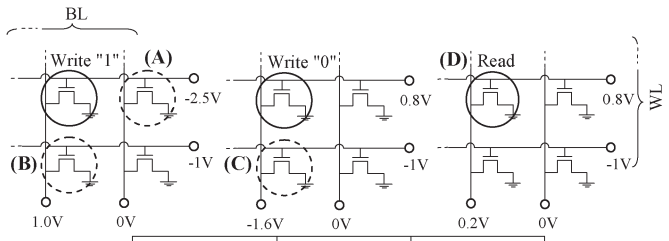


Fig. 8. Transient analysis of the 1T-DRAM cell using GIDL current. Data can be written and read within several nanoseconds.

the drain, and the body, according to each operating voltage. Data can be written and read within several nanoseconds. This verifies that the 1T DRAM using GIDL current can operate under all of the memory conditions. It is very important to consider disturb margins for selective read and write operations in a DRAM. All disturb conditions are summarized in Fig. 9. The "1" disturb means that stored data in a cell becomes "1" from "0," and "0" disturb means that stored data becomes "0" from "1."

A. "1" Disturb

Fig. 10 shows the relationship between the "1" write time and the gate voltage with different drain voltages for a "0" stored cell. Since a gate voltage of −1.0 V and a drain voltage of 0 V



	"1" disturb		"0" disturb	
Cell	(A)	(B)	(C)	(D)
Gate voltage (V)	-2.5	-1.0	-1.0	0.8
Drain voltage (V)	0	1	-1.6	0.2

Fig. 9. Worst case of disturbance in the memory function. The "1" disturb means that stored data in a cell becomes "1" from "0." The "0" disturb means that stored data in a cell becomes "0" from "1."

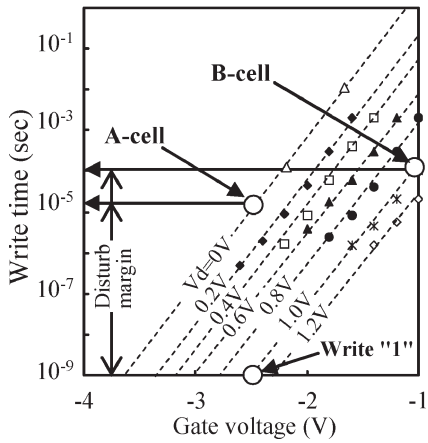


Fig. 10. Relationship between the "1" write time and the gate voltage with different drain voltages for a "0" stored cell.

are applied during the hold state, the "1" write time for a "0" stored cell is more than 1 s, which means "0" retention time is more than 1 s in case there is no disturbance. Bias conditions for both A and B cells are indicated. The gate voltage of the target cell was −2.5 V, and the drain voltage was 1 V. Bias conditions for both A and B cells are indicated. The gate voltage of the target cell was −2.5 V, and the drain voltage was 1 V. When "1" was written to the target cell, a gate voltage of −2.5 V and a drain voltage of 0 V was applied to the A cell, and a gate voltage of −1.0 V and a drain voltage of 1.0 V was applied to the B cell. Under those conditions, the data stored in A and B cells were forced to change from "0" to "1" because of GIDL-based hole generation. While it is about 1 ns for the write "1" operation, the "1" write times for A and B cells are more than 10 and 100 μs, respectively. These are identical to the "1" disturb time margin of more than four digits.

B. "0" Disturb

Fig. 11 shows "1" retention characteristics for the C cell. First, we wrote "1" to the C cell; then, we could read "1" from the cell. Then, we wrote "0" to the target cell with a gate voltage of 0.8 V and a drain voltage of −1.6 V. When "0" was written to the target cell, a gate voltage of −1.0 V and a drain voltage of −1.6 V were applied to the C cell. The longer the write "0"

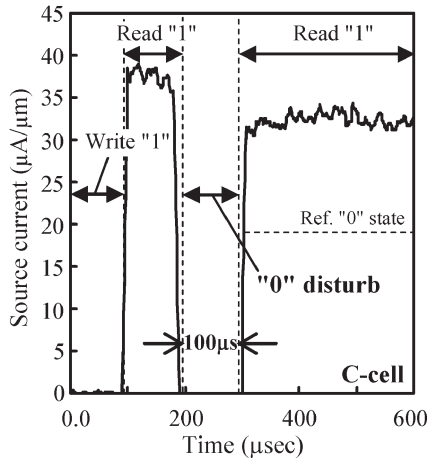


Fig. 11. Data "1" retention characteristics for the C cell. Data "1" can be read for the C cell even after the "0" disturb time of 100 μs.

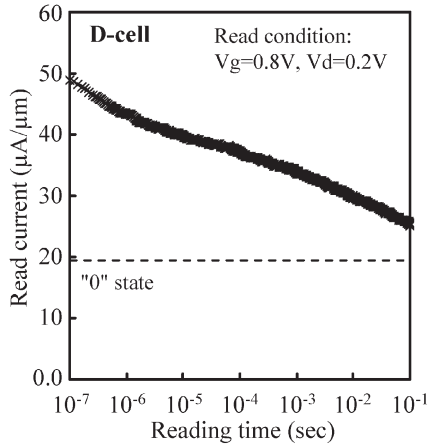


Fig. 12. Relationship between the read "1" current and the read time. Data "1" can still be read after 1 ms.

time, the lower the source current of the C cell for reading "1." This is because of a lack of accumulated holes for the C cell caused by the forward bias of the p-n junction, which consists of the drain and the body.

Data "1" can be read for the C cell even after the "0" disturb period of 100 microseconds. This is because the "hold" gate voltage of -1.0 V keeps the body voltage low and suppresses the escape of holes from the body. This leads to the conclusion that the "hold" gate voltage of -1.0 V is sufficient for the "0" disturb time margin of 100 μs.

Fig. 12 shows the relationship between the read current and the read time for the D cell. As the read time becomes longer, the read current gradually decreases because of the lack of holes. We defined the retention time of the memory as the time that is 50% charge loss. Data "1" can still be read after 1 ms. After all, there are enough disturb margins for each operation in the 1T DRAM using GIDL current.

V. Conclusion

Considering the capacity, the speed, and the structural complexity of an embedded memory, a capacitorless 1T DRAM seems the most promising. By using the GIDL current to write the "1" state, the drain current can be lowered remarkably, compared with that using II current. Compared with use of II current, the use of GIDL current in write "1" operation achieves power consumption that is lower by four orders of magnitude, which leads to an operative power reduction. Using GIDL current, the capacitorless 1T DRAM can read and write within several nanoseconds and has a larger sense margin than when using II current due to an increase in the number of accumulated holes, which is caused by a negative body potential in the write operation. As for the memory function, the disturb margin, which is important for the selective read and write operation, is discussed in detail, and it is shown that the 1T DRAM using GIDL current has enough disturb margins for each operation. Thus, the 1T DRAM using GIDL current should be a very promising embedded memory for low-power and high-speed systems-on-a-chip.

Acknowledgment

The authors would like to thank M. Matsumiya and S. Eto for their helpful discussions and M. Kase and J. Sakuma for the device fabrication.

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